

regions 34. The n<sup>+</sup>-type regions 36a and 36b serve as source and drain regions of the depletion type lateral MOS field effect transistor in the p-well region 25. The n<sup>+</sup>-type regions 36c and 36d serve as source and drain regions of the enhancement type lateral MOS field effect transistor in the p-well region 25. The n<sup>+</sup>-type regions 36e serve as source regions of the vertical MOS field effect transistors in the n<sup>-</sup>-type epitaxial layer 23. An inter-layer insulator 37 is entirely formed over the gate electrodes 30a, 30b and 30c, and the gate electrodes 29a, 29b and 29c as well as over the field oxide films 26. Yet another resist film is entirely applied over the inter-layer insulator 37. The resist film is then patterned by a lithography technique to form a resist pattern with openings which are positioned over contact regions of the inter-layer insulator 37.--.

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Cont

(Page 6, replace the paragraph, beginning on line 5, as follows: ]

--With reference to FIG. 1J, the resist pattern 38 is used as a mask for selectively etching the inter-layer insulator 37 and the gate oxide films 29a, 29b and 29c to form contact holes in the inter-layer insulator 37. The contact holes are positioned over the n<sup>+</sup>-type regions 36a, 36b, 36c and 36d, as well as over the p<sup>+</sup>-type regions 34 and the n<sup>+</sup>-type regions 36e, whereby parts of the n<sup>+</sup>-type regions 36a, 36b, 36c and 36d as well as the p<sup>+</sup>-type regions 34 and parts of the n<sup>+</sup>-type regions 36e are exposed through the contact holes in the inter-layer

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insulator 37. The used resist pattern 38 is completely removed. An aluminum layer 39 is entirely formed over the inter-layer insulator 37 and within the contact holes, so that the aluminum layer 39 is in contact with the parts of the n+-type regions 36a, 36b, 36c and 36d as well as the p+-type regions 34 and the parts of the n+-type regions 36e. A resist film is further applied entirely over the aluminum layer 39. The resist film is then patterned by a lithography technique to form a resist pattern 40.--.

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Page 21, replace the paragraph, beginning on line 9, as follows:

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--With reference to FIG. 2I, the resist pattern 13 is used as a mask for selective ion-implantation of boron as a p-type impurity into the p-type regions 12 at a high impurity concentration. The resist pattern 13 is completely removed. A heat treatment is then carried out at 1000° C for a several tens minutes for activation of the implanted impurity to selectively form p+-type regions 14 in the p-type regions 12. The p+-type regions 14 are higher in impurity concentration than the p-type regions 12. The p+-type regions 14 serve to suppress effective operations of parasitic bipolar transistors to the vertical MOS field effect transistors. Still another resist film is entirely applied over the gate electrodes 10a, 10b and 10c, and the gate electrodes 9a, 9b and 9c as well as over the field oxide films 7a. The resist film is then patterned by a lithography technique

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to form resist patterns 15 which are positioned over the p+-type regions 14.--.

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Page 23, replace the paragraph, beginning on line 9, bridging pages 23 and 24, as follows:

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--With reference to FIG. 2L, the resist pattern 20 is used as a mask for selectively etching the aluminum layer 19 to form aluminum electrodes 19a, 19b, 19c, 19d, and 19e. The aluminum electrodes 19a and 19b are in contact with the source and drain regions 16a and 16b of the depletion type lateral MOS field effect transistor in the p-well region 5, so that the aluminum electrodes 19a and 19b serve as source and drain electrodes of the depletion type lateral MOS field effect transistor. The aluminum electrodes 19c and 19d are in contact with the source and drain regions 16c and 16d of the enhancement type lateral MOS field effect transistor in the p-well region 5, so that the aluminum electrodes 19c and 19d serve as source and drain electrodes of the enhancement type lateral MOS field effect transistor. The aluminum electrode 19e is in contact with the p+-type regions 14 and the parts of the n+-type regions 16e in the p-type regions 12, so that the aluminum electrode 19e serves as a source electrode of the vertical MOS field effect transistor. The used resist pattern 20 is completely removed. A bottom electrode 21 is formed on a bottom surface of the semiconductor substrate 1.--.

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